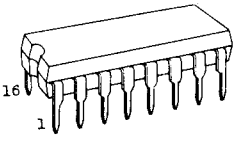
TC5064BP, TC5065BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC5064BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/NON INVERTING TYPE
TC5065BP HEX HIGH VOLTAGE BUFFER WITH INHIBIT/INVERTING TYPE

TC5064BP and TC5065BP contain six circuits of buffers having two common INHIBIT inputs (A_{IN}, $\overline{B_{IN}}$).
As both have the output of open drain structure with high bleakdown voltage P-channel MOS FET (-50 volts.. ... Maximum Rating), these are suitable for driving fluorescent display tubes and for interfacing with high voltage MOS LSI's.
TC5064BP is non-inverting type and TC5065BP is inverting type.

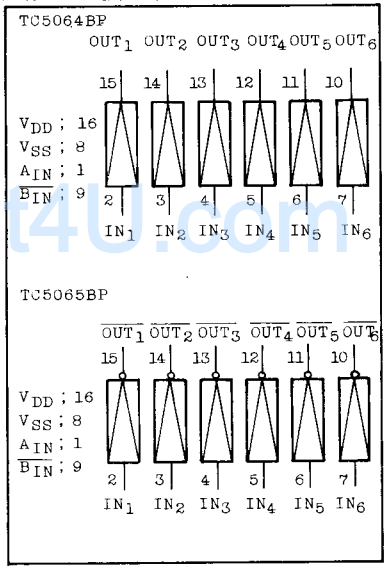


DIP 16 (3D16A-P)

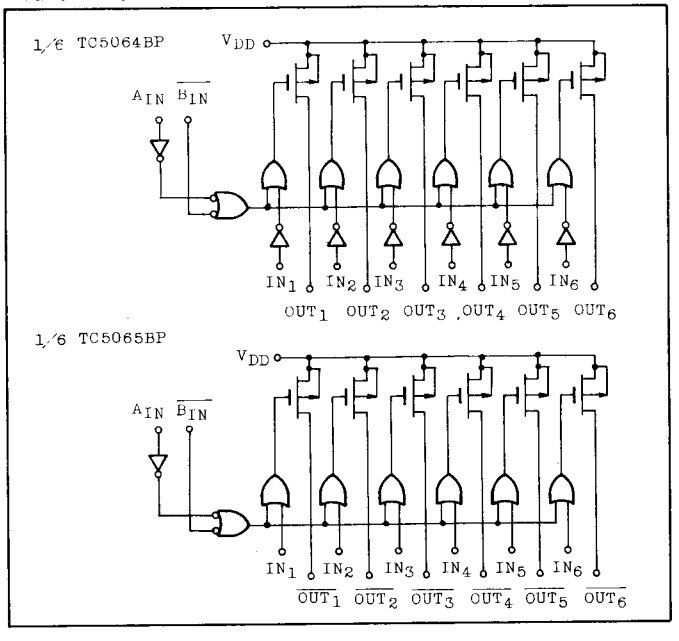
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{DD}-50 ~ V_{DD}+0.5	V
Power Dissipation	P_D	300	mW
DC Input Current	I_{IN}	±10	mA
Storage Temperature Range	T_{stg}	-65 ~150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	
A_{IN}	$\overline{B_{IN}}$	IN	TC5064BP	TC5065BP
L	H	L	HZ	H
L	H	H	H	HZ
*	L	*	HZ	HZ
H	*	*	HZ	HZ

HZ ; High Impedance
* ; Don't care

RECOMMENDED OPRATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3		18	V
Input Voltage	V_{IN}		0		V_{DD}	V
Operating Temp.	Topr		-40		85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

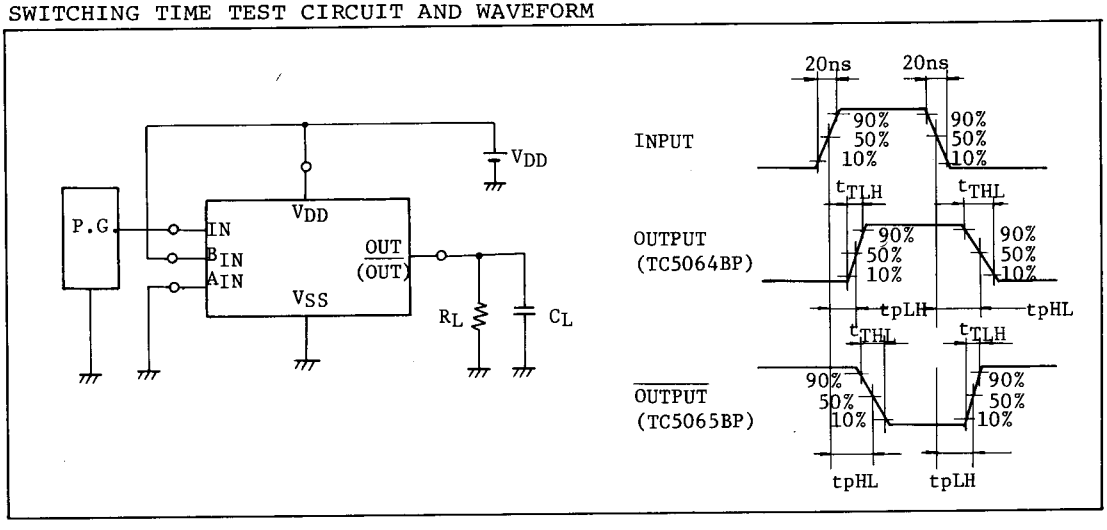
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High Level Output Voltage	V_{OH}	$\|I_{OUT}\| < 1\mu A$ $V_{IN}=V_{SS}$ or V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
High Levle Output Current	I_{OH}	V_{OH}=3V (V_{DD}-2V)	5	- 6	-	- 5	-10	-	- 4	-	mA
		V_{OH}=2V (V_{DD}-3V)	5	- 9	-	- 8	-13	-	- 6	-	
		V_{OH}=7V (V_{DD}-3V)	10	-12	-	-10	-25	-	- 8	-	
		V_{OH}=12V(V_{DD}-3V)	15	-17	-	-15	-35	-	-12	-	
High Level Input Voltage	* V_{IH}	V_{OUT}=0.5V,4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V,9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.5	-	
Low Level Input Voltage	* V_{IL}	V_{OUT}=0.5V,4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V,9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
Output OFF Current	I_{OFF}	V_{OUT} = 0V	15	-	- 3	-	-0.01	-3	-	-10	μA
		V_{OUT} = VDD-45V	15	-	- 10	-	-1	-10	-	-20	
Input Current	I_{IH}	V_{IH} = 18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	I_{IL}	V_{IL} = 0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Supply Current	I_{DD}	$V_{IN}=V_{SS}$, V_{DD}, OUTPUTS OPEN	5	-	4.0	-	0.005	4.0	-	30	μA
			10	-	8.0	-	0.010	8.0	-	60	
			15	-	16.0	-	0.015	16.0	-	120	

* R_L = 20 kΩ

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

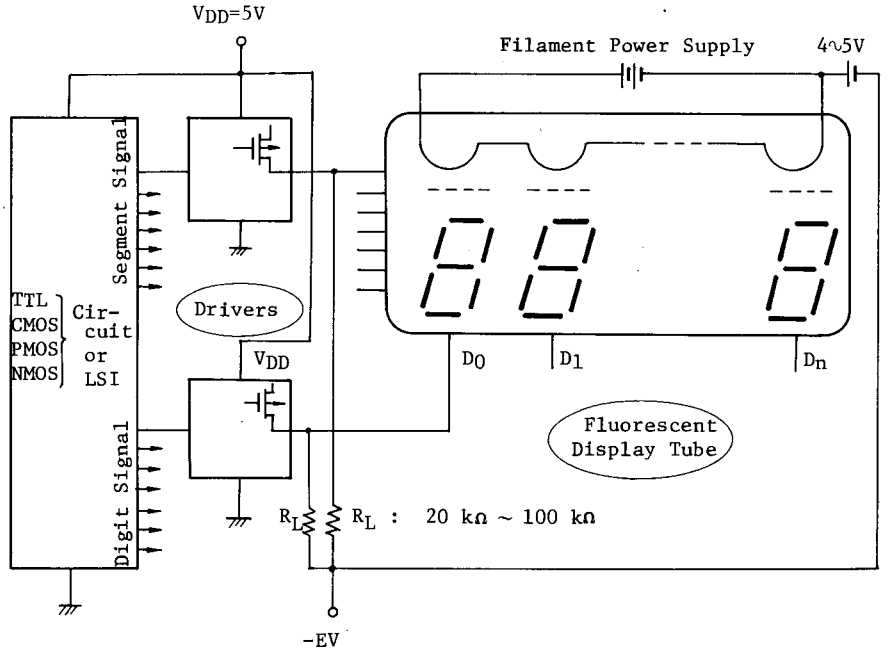
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Rise Time	t_{TLH}	R_L = 20 kΩ	5	-	100	200	ns
			10	-	50	100	
			15	-	40	80	
Output Fall Time	t_{THL}	R_L = 20 kΩ	5	-	5.0	8.0	μs
			10	-	5.0	8.0	
			15	-	5.0	8.0	
(LOW-HIGH) Propagation Delay Time	t_{pLH}	R_L = 20 kΩ	5	-	200	500	ns
			10	-	100	250	
			15	-	80	200	
(HIGH-LOW) Propagation Delay Time	tpHL	R_L = 20 kΩ	5	-	2.0	4.0	μs
			10	-	2.0	4.0	
			15	-	2.0	4.0	
Input Capacity	C_{IN}				5	7.5	pF

SWITCHING TIME TEST CIRCUIT AND WAVEFORM



EXAMPLES OF APPLICABLE CIRCUITS

(1) Fluorescent Display Tube Driving Circuit



(2) Interface between CMOS and PMOS